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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,826	01/04/2001	Charles W. Pearce	PEARCE 26	5388

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HITT GAINES, PC
LSI Corporation
PO BOX 832570
RICHARDSON, TX 75083

EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	09/755,826	PEARCE, CHARLES W.	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over D'Anna et al., U.S./5,841,166.

Re claim 1, D'Anna et al. disclose a method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, which comprises forming a lightly-doped source/drain region 46 (fig. 3A) with only a first dopant (i.e., Arsenic, col. 2, lines 55-60), the lightly-doped source/drain region *formed* between first and second isolation structures 52/54 etc. (figs. 3A-3B); and creating a gate 58 (fig. 3B) over the lightly-doped source/drain region, see figs. 1A-4 and cols. 1-4 for more details.

Re claim 2, wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant (col. 2, lines 56-60).

Re claim 3, wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm.sup.2 to about 1E13 atoms/cm.sup.2 (i.e., 5E12 col. 2, lines 56-60).

Re claim 4, wherein the first N-type dopant has an implant dose of about 5E12 atoms/cm.sup.2 (i.e., 5E12 col. 2, lines 56-60).

Re claim 5, further including diffusing a second dopant (i.e., boron; col. 3, lines 8-18) at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel (fig. 3C).

Re claim 6, wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm.sup.2 to about 1E14 atoms/cm.sup.2 (i.e., 1E13; col. 3, lines 8-18).

Re claim 7, wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an implant dose of the first dopant (in this case, the p-type dopant having an implant dose of about 5E14 and the fist dopant of about 5E12, also see col. 2, lines 56-60 and col. 3, lines 8-16).

Re claim 8, further including placing a heavy concentration of the first dopant (i.e., arsenic; col. 3, lines 16-18) in a region adjacent a source side of the gate (fig. 3D), and in the lightly-doped source/drain region adjacent a drain side of the gate (fig. 3D).

Re claim 10, wherein placing includes placing an implant dose of the first dopant ranging from about 1E15 atoms/cm.sup.2 to about 1E16 atoms/cm.sup.2 (i.e., 1E15-1E16; col. 3, lines 16-18).

Re claim 11, D'Anna et al. disclose a method of manufacturing an integrated circuit, comprising: fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors (i.e., col. 1, lines 5-10), including: forming a lightly-doped source/drain region 46 (fig. 3A) with only a first dopant (i.e., Arsenic, col. 2, lines 55-60), the lightly-doped source/drain region formed between first and second isolation structures 52/54 etc. (figs. 3A-3B); and creating a gate 58 (fig. 3B) over the lightly-doped source/drain region; depositing interlevel dielectric layers (fig. 3D;

col. 3, lines 19-28) over the LDMOS transistors; and creating interconnect structures (i.e., source contact, drain contact etc.) in the interlevel dielectric layers and interconnecting the LDMOS transistors to form an operative-integrated circuit (figs. 3D-4; col. 3, lines 19-55), see figs. 1A-4 and cols. 1-4 for more details.

Re claim 12, wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant (col. 2, lines 56-60).

Re claim 13, wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm.sup.2 to about 1E13 atoms/cm.sup.2 (i.e., 5E12 col. 2, lines 56-60).

Re claim 14, wherein the first N-type dopant has an implant dose of about 5E12 atoms/cm.sup.2 (i.e., 5E12 col. 2, lines 56-60).

Re claim 15, further including diffusing a second dopant (i.e., boron; col. 3, lines 8-18) at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel (fig. 3C).

Re claim 16, wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm.sup.2 to about 1E14 atoms/cm.sup.2 (i.e., 1E13; col. 3, lines 8-18).

Re claim 17, wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an implant dose of the first dopant (in this case, the p-type dopant having an implant dose of about 5E14 and the fist dopant of about 5E12, also see col. 2, lines 56-60 and col. 3, lines 8-16).

Re claim 18, further including placing a heavy concentration of the first dopant (i.e., arsenic; col. 3, lines 16-18) in a region adjacent a source side of the gate (fig. 3D), and in the lightly-doped source/drain region adjacent a drain side of the gate (fig. 3D).

Re claim 20, wherein placing includes placing an implant dose of the first dopant ranging from about 1E15 atoms/cm.sup.2 to about 1E16 atoms/cm.sup.2 (i.e., 1E15-1E16; col. 3, lines 16-18).

D'Anna et al. disclosed above; however, D'Anna et al. does not explicitly show the particular order to the steps (i.e., forming isolation structures before the step of forming LDD). With respect to the order of process steps: Selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable process sequence for forming the device as taught by D'Anna et al.

Re Claims 9 and 19, D'Anna et al. disclosed in above, and in particular figs. 3C-4 show that there is distance/space between the drain N+ and the gate. However, D'Anna is silent to the range as recited in the instant claims 9 and 19. With respect to claimed ranges of the distance/space, absent evidence of disclosure of criticality for the range giving unexpected results are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller 105 USPQ233, 255 (CCPA 1955)*, the selection of reaction parameters such as thickness, distance, temperature and concentration etc. would have been obvious. *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70*

USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable distance in the method of D'Anna et al. in order to provide normal operation for the MOS under the high voltage.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed process/arrangement/order of steps (i.e. – the order of the steps and the claimed ranges of the distance) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

3. Claims 1-3 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosiak et al., U.S./4,918,026.

Re claim 1, Kosiak et al. disclose a method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, which comprises forming a lightly-doped source/drain region 114 (figs. 1 and 2B; col. 2, lines 63-66) with only a first dopant (i.e., phosphorous, col. 4, lines 32-39), the lightly-doped source/drain region formed between first and second isolation structures 50/120 etc. (fig. 1); and creating a gate 118 (fig. 1) over the lightly-doped source/drain region, see figs. 1-2G and cols. 1-10 for more details.

Re claim 2, wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant (col. 4, lines 32-39; i.e., phosphorus).

Re claim 3, wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm.sup.2 to about 1E13 atoms/cm.sup.2 (i.e., 4.5E12, col. 4, lines 32-39).

Re claim 11, Kosiak et al. disclose a method of manufacturing an integrated circuit, comprising: fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors (also see col. 3, line 63 to col. 4, line 10 regarding transistors), which includes forming a lightly-doped source/drain region 114 (figs. 1 and 2B; col. 2, lines 63-66) with only a first dopant (i.e., phosphorous, col. 4, lines 32-39), the lightly-doped source/drain region formed between first and second isolation structures 50/120 etc. (fig. 1); and creating a gate 118 (fig. 1) over the lightly-doped source/drain region; depositing interlevel dielectric layers (i.e., PSG, SOG, etc., col. 7, lines 30-62) over the LDMOS transistors; and creating interconnect structures (i.e., metal contacts, etc., col. 7, lines 30-62) in the interlevel dielectric layers and interconnecting the LDMOS transistors to form an operative-integrated circuit, see figs. 1-2G and cols. 1-10 for more details.

Re claim 12, wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant (col. 4, lines 32-39; i.e., phosphorus).

Re claim 13, wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm.sup.2 to about 1E13 atoms/cm.sup.2 (i.e., 4.5E12, col. 4, lines 32-39).

Kosiak et al. disclosed above; however, Kosiak et al. does not explicitly show the particular order to the steps (i.e., forming isolation structures before the step of forming LDD). With respect to the order of process steps: Selection of any order of performing process steps is

prima facie obvious in the absence of new or unexpected results In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable process sequence for forming the device as taught by Kosiak et al. Furthermore, the specification contains no disclosure of either the critical nature of the claimed process (i.e. – the order of the steps) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (8:00am-4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jack Chen
Primary Examiner
Art Unit 2813

/Jack Chen/
Primary Examiner, Art Unit 2813